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2-D IIR Spatially Bandpass Beam Filter- A Multiplierless Realization

Siji P .V[1], Manju Manuel[2]

Department of Electronics and Communication Engineering, Rajiv Gandhi Institute of Technology, Kottayam, India[1,2]

Abstract: The 2-D IIR Spatially Bandpass (SBP) beam filters are used for directional filtering of temporally broadband bandpass space time plane waves. These filters have applications in radio astronomy, seismic signal processors, radar navigation, space science and wireless communications. If filter coefficients are represented in Canonic Signed Digit (CSD) space, the multiplier circuit can be replaced with adders/ subtractors and shifters. In this paper, a multiplierless realization of 2D IIR SBP beam filter is proposed and the realization is done on Zedboard xc7z020. Multiplierless 2-D IIR SBP beam filter has low complexity compared to 2D IIR SBP beam filter. Circuit complexity analysis is also presented.

Keywords: Zedboard, CSD representation, System Generator, 2D IIR SBP beam filter.

I. INTRODUCTION

Beamforming applications require spatio temporal plane wave filters. The term beamforming refers to selective enhancement of desired broadband spatio-temporal (ST) plane waves based on their direction of arrivals (DOAs) [3]. 2-D IIR frequency planar beam filter is an example of spatio temporal plane wave filter [2]. Spatial modulation of first order 2-D IIR frequency planar beam filter results a second order 2-D IIR spatially bandpass (SBP) beam filter. These filters are used for filtering temporally-broadband bandpass signals.

In real time hardware implementation, speed of operation is an important factor. The systolic array architecture is commonly used for hardware implementation of 2D space-time filters. The systolic array based spatio-temporal plane wave filter has a throughput of one frame per clock cycle and much lower critical path delays [4].

The multipliers are the most power consuming circuits and occupy large silicon area. If we replace multipliers with some other alternatives, we can save both area and power. Signed Power of Two (SPT) representation is an efficient way for replacing multipliers. Removing the multipliers is equivalent to reducing the circuit complexity and minimizing the power dissipation and chip area.

Among various Signed Power of Two representation, Canonic signed digit (CSD) representation [5] is minimal, uses both additions and subtractions, and this will give minimum number of SPT terms with precision. A multiplierless 2-D IIR SBP beam filter can be designed by representing filter coefficient in CSD space. Multiplierless 2-D IIR SBP beam filter consumes less chip area and power than 2-D IIR SBP filter as filter coefficients are represented in CSD space.

In this paper realization of a multiplierless 2D IIR SBP beam filter is proposed. The hardware realization of filter is proposed on Zedboard xc7z020. The design is synthesized using Vivado 2014.4 design tools, Xilinx System Generator and MATLAB/Simulink.

This paper is organized as follows: A review of 2D IIR spatially bandpass beam filter is given in section I. Section II presents the proposed design of multiplierless 2D IIR beam filter. Description about hardware realization of filter which includes details of Zedboard, System Generator design of filter is given in section III. Simulation results and Hardware co-simulation test results are described in section IV. Finally, the paper is concluded in section V.

A. Review of 2D IIR SBP Beam Filters

The 2D IIR Spatially Bandpass (SBP) beam filters [1] are mainly used for the selective enhancement of desired temporally broadband spatially bandpass space-time plane waves. It is an extension of 2D IIR frequency planar beam filter [2] and the impulse response of SBP filter is obtained by applying spatial modulation to the impulse response of 2D IIR frequency planar beam filter. The transfer function of 2D IIR SBP filter is given as [1],

$$H_B(z_1, z_2) = \frac{Y(z_1, z_2)}{W(z_1, z_2)}$$

$$= \frac{\sum_{i=0}^{2}\sum_{j=0}^{2} a_{ij}\, z_1^{-i} z_2^{-j}}{1+\sum_{i=0}^{2}\sum_{j=0}^{2} b_{ij}\, z_1^{-i} z_2^{-j}} (1 + z_2^{-1}) \qquad (1)$$

Where, a_{ij} and b_{ij} are filter coefficients [1]. The inverse Z transform of (1) gives 2D input-output difference equation.

This 2D input-output difference equation is used for the design of Parallel processing core (PPCM) modules in systolic array architecture [1].

Fig. 1 shows the block diagram of PPCM of 2D IIR SBP beam filter. The PPCM computes one sample per clock cycle. The filter circuit is realized by cascading these PPCMs.

Fig. 2. shows the systolic array based 2D IIR SBP beam filter used in linear sensor array based applications.

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II. PROPOSED MULTIPLIERLESS 2D IIR SBP BEAM FILTER

In this paper, the design of a multiplierless 2D IIR SBP beam filter is proposed. The multiplierless design is done by representing filter coefficients in Canonic Signed Digit (CSD) space. Multiplierless 2-D IIR SBP beam filter consumes less chip area and power than 2-D IIR SBP filter as filter coefficients are represented in CSD space.

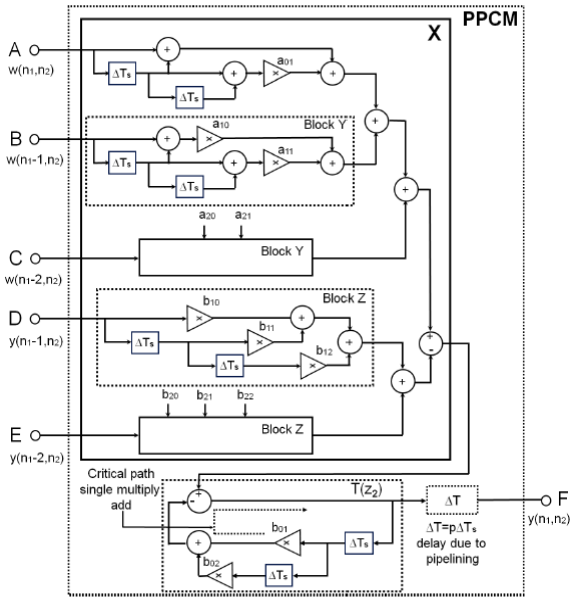

Fig. 1. Block diagram of a PPCM of 2D IIR SBP beam filter [1]

A. Canonic Signed Digit Representation

The canonic signed digit (CSD) code is a ternary number system. The symbol set used in CSD is [1, 0,−1]. It is a minimal representation that is, the CSD representation of a number contains minimum number of nonzero digits. A number can be represented in CSD space as [2],

$$q = \sum_{i=1}^{w} d_i \, 2^{R-i} \qquad (2)$$

Where, w is the word length of the CSD number d_1, d_2, d_3,…..d_w. R determines the position of radix point. The CSD representation has two properties:

1) $d_i d_{i-1} = 0$ (canonic property),
2) the CSD representation of a number is unique.

B. Design and Hardware Realization of Proposed Multiplierless 2D IIR SBP Beam Filter

Multiplierless 2-D IIR SBP beam filter is realized by representing filter coefficients in CSD space. Table 1 shows CSD representation of filter coefficients used in the design of 2D IIR SBP beam filter. Fig. 3 shows the internal diagram of PPCM of proposed multiplierless 2-D IIR SBP beam filter.

The CSD multipliers made from shifters, adders and subtractors are used to replace each filter coefficient multiplier. The design is synthesized in vivado 2014.4 Xilinx System Generator design tool and the hardware realization is done on Zedboard xc7z020.

TABLE I: FILTER COEFFICIENTS IN CSD FORMAT

Filter coefficients	CSD representation	No: of adders
0.37460029162112	010-10000000-10010	3
0.5311118922	0100010000000-100	2
-0.3533368573	0-101010-100000000	3
0.24889435893804	00-10000000100100	2
-0.8742940673169	-100100000010-1000	3
0.7492005832	10-10000000-101000	3
0.1403253785	000100100000-1000	3
-0.351989778	0-10101010-100000000	3
-1.368294001	-1000000000000000	1
-0.463170233	0-10001010-1000000	3

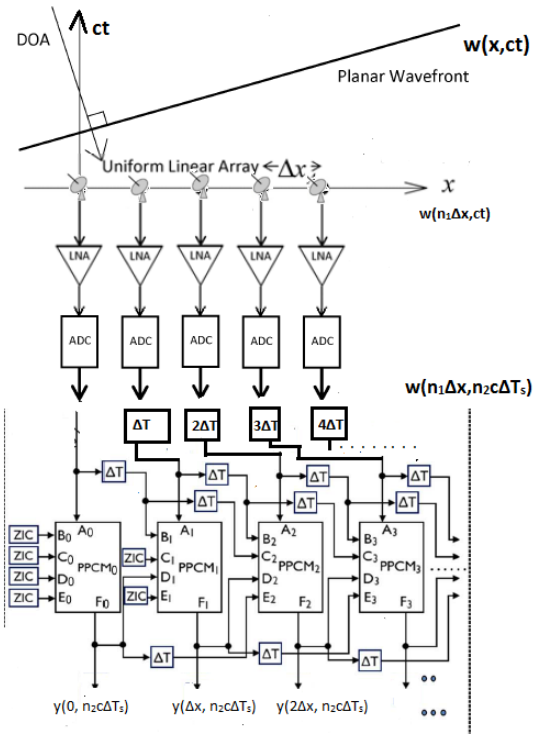

Fig. 2. Systolic array based 2D IIR SBP beam filter

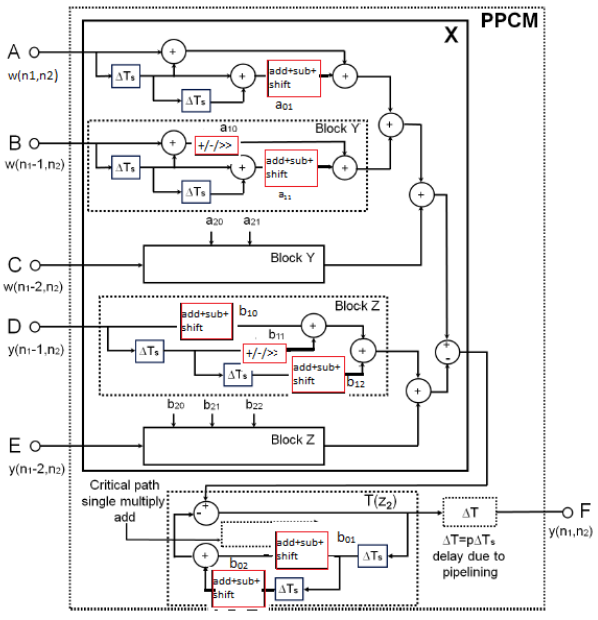

Fig. 3. Block diagram of PPCM of proposed multiplierless 2D IIR SBP beam filter

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C. Zedboard

The Zedboard integrates a feature-rich dual-core ARM Cortex A9 MP Core based processing system(PS) and Xilinx programmable logic (PL) in a single device, built on a state-of-the-art, high-performance, low-power (HPL), 28 nm, and high-k metal gate (HKMG) process technology. The ARM Cortex-A9 MP Core CPUs are the heart of the PS which also includes on-chip memory, external memory interfaces, and a rich set of I/O peripherals.

The Zedboard offers the flexibility and scalability of an FPGA, while providing performance, power, and ease of use typically associated with ASIC. This device enables designers to target cost-sensitive as well as high-performance applications from a single platform using industry-standard tools. The integration of the PS with the PL provides levels of performance that two chip solutions (for example, an ASSP with an FPGA) cannot match due to their limited I/O bandwidth, loose coupling and power budgets. Fig. 4 shows the image of zedboard xc7z020.

Once the simulation is verified, a hardware co-simulation block along with bitstream file is generated. For FPGA realization, this bitstream file is used. The PPCM block and the 2nd order multiplierless 2D IIR SBP beam filter consisting of N = 5 PPCMs have been implemented on Xilinx Zedboard xc7z020. The operation of the beam filter is verified by exciting the inputs of the filter by a 2D unit impulse function and measuring the impulse response from the onchip realizations. Fig. 5 shows the hardware co-simulation block of proposed 2D IIR SBP beam filter employing 5 PPCMs.

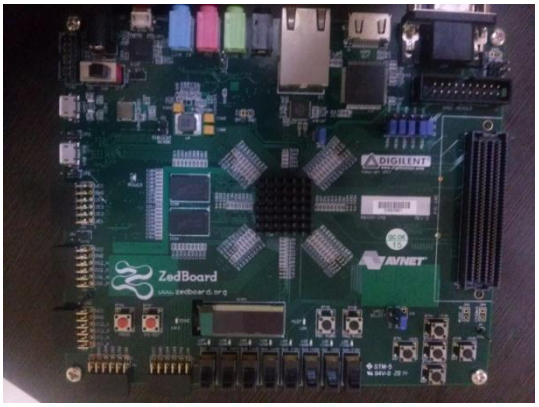

Fig. 4. Zedboard xc7z020

III. RESULTS

The circuit is designed in 2's complement fixed-point binary arithmetic with W = 16 and D = 12(where W is the word length and D is the position of binary point). The input signal used is 2-D unit impulse function.

A. Hardware Co-simulation Test Results

Fig. 6 shows the impulse responses of 2-D IIR SBP beam filter and fig.7 shows the impulse response of multiplierless 2D IIR SBP beam filter obtained from onchip realizations. The PPCM0 outputs of both filters look similar. The PPCM5 output of multiplierless 2-D IIR SBP beam filter has slight variations with that of 2-D IIR SBP beam filter. These varia-ations are due to the quantization noise effects in canonic sig-ned digit representation. There are various optimization tech-niques to reduce these quantization noise. Table II presents the impulse responses of filters.

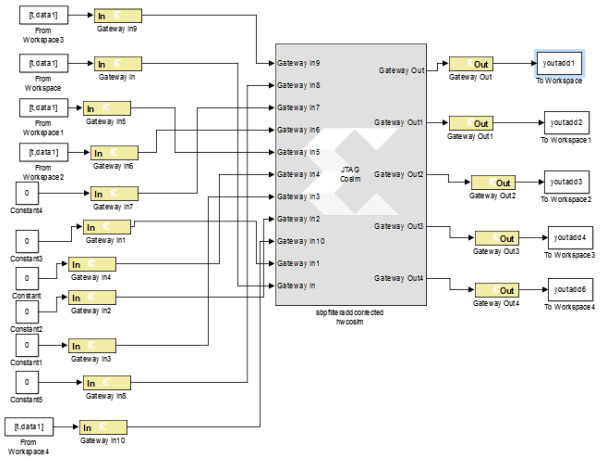

Fig. 5. Hardware co-simulation block of proposed multiplierless 2D IIR SBP beam filter

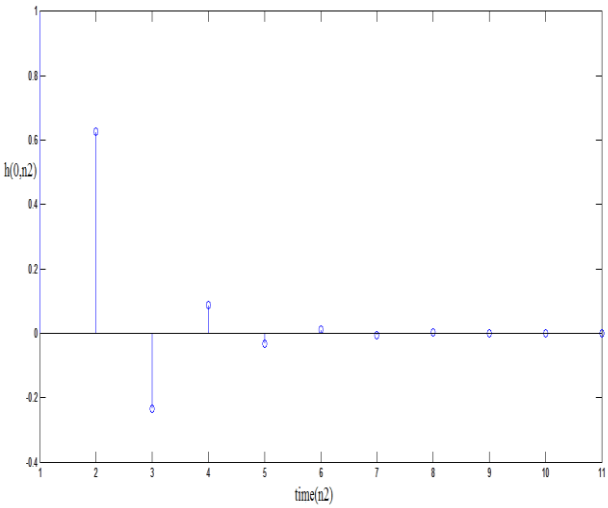

Fig. 6. Output of PPCM0 of 2-D IIR SBP beam filter when excited input by 2-D impulse input function

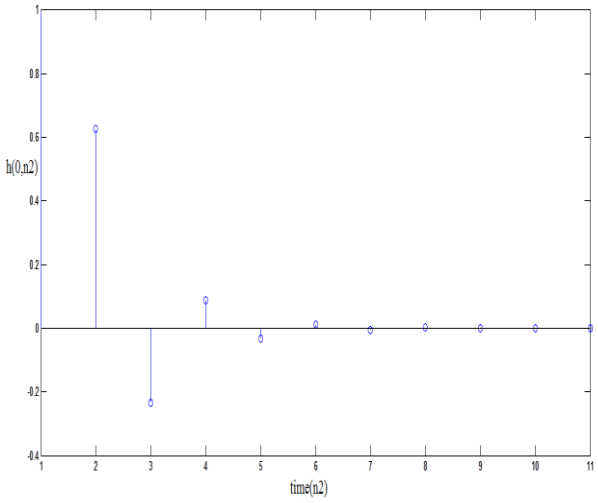

Fig. 7. Output of PPCM0 of proposed multiplierless 2-D IIR SB beam filter when excited input by 2-D impulse input function

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TABLE II: IMPULSE RESPONSES OF FILTERS

Impulse response of PPCM0 of 2D IIR SBP beam filter (h(0,n2))	Impulse response of PPCM0 of proposed multiplierless 2D IIR SBP beam filter (h(0,n2))
1	1
0.6254	0.6253
-0.2343	-0.2341
0.0878	0.0878
-0.0329	-0.0330
0.0124	0.0125
-0.0046	-0.0047
0.0018	0.0018
-6.1035e-04	-6.7139e-04
2.4414e-04	3.0518e-04
0	-1.2207e-04

B. Comparison on Area Utilization

This section presents a comparison of both filter in terms of logic utilization. There has been a reduction of 16 LUTs per PPCM in multiplierless 2D IIR SBP filter. Table III presents the comparison results of 2D IIR SBP beam filter and multiplierless 2D IIR SBP beam filter interms of number of LUTs used.

TABLE III: COMPARISON OF NUMBER OF LUTS USED

Filter coefficient	2D IIR SBP beam filter(No: LUTs used)	Multiplierless 2D IIR SBP beam filter (No: LUTs used)
b11	70	23
b01	60	45
a10	56	47
a21	49	44
a20	45	38
b20	44	19
b10	66	70
b12	60	68
a11	58	70
a01	56	72
b21	56	72
b02	52	73
b22	52	73
Total	730	714

IV. CONCLUSION

A multiplierless 2-D IIR SBP beam filter was implemented on Zedboard xc7z020. The 2D IIR SBP beam filter is used for spatio temporal plane wave filtering of bandpass signals. Applications for these filters are emerging in diverse areas such as steerable smart antenna arrays, ultrasonic imagers, seismic signal processors, and directional audio systems. The proposed multiplierless 2D IIR SBP beam filter is designed by representing filter coefficient in CSD space. The CSD representation allows the multiplications to be replaced by shift add and subtraction operations, which reduces circuit complexity and power consumption.

For hardware realization, systolic array architecture is used. The synthesis of the design is done using Matlab/Simulink, Xilinx System Generator (XSG) and the Vivado 2014.4 design tools. Simulation results and hardware cosimulation test results are also presented. The proposed Multiplierless 2D IIR filter has low complexity (16 LUT reduction per PPCM)compared to 2D IIR SBP beam filter. Future prospects include the analysis of quqntization error and techniques for minimizing it along with the reduction of computation complexity.

REFERENCES

[1] Rimesh. M.Joshi, A.Madanayake and L. T. Bruton, "Synthesis and array processor realization of a 2-D IIR beam filter for wireless applications," *IEEE Trans. On very large scale integra.I, Reg. Papers, votion systems*, vol.20. Dec.2012.

[2] A. Madanayake and L. T. Bruton, "A speed-optimized systolic array processor architecture for spatio-temporal 2-D IIR broadband beam filters," *IEEE Trans. Circuits Syst. I, Reg Papers*,vol. 55, no. 7, pp. 1953–1966, Aug. 2008.

[3] S. V. Hum, A. Madanayake, and L. T. Bruton, "UWB beamforming using 2D beam digital filters," *IEEE Trans. Ant. Propag. (TAP)*, vol.57, no. 3, pp. 804–807, Mar. 2009.

[4] A. Madanayake and L. T. Bruton, "A real-time systolic array processor implementation of two-dimensional IIR filters for radio-frequency smart antenna applications," *in Proc. IEEE Int. Symp. Circuits Syst.(ISCAS)*, 2008, pp. 1252–1255.

[5] Z. Tang, J. Zhang, and H. Min, "A High-Speed, Programmable, CSD Coefficient FIR Filter," *Transactions on Consumer Electronics*, Vol. 48, No. 4, pp. 834-837, 2002.